International
Journal
Of Advanced Research in Engineering & Management (IJAREM)

Leakage Power Reduction Using Power Gated Sleep Method

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ABSTRACT: Now a day's low power circuits are most popular, in the circuit as the scaling increase the leakage powers increases. So for removing these kinds of leakages we are using many types of power gating techniques and to provide a better power efficiency. In this paper by using low power VLSI design techniques we are going to analyze the different types of power gated circuits. We are going to display the comparison results between different nano-meter technologies. Micro-wind Layout Editor & DSCH software tools are used for simulations & circuit design. The results were tabulated.
Keywords **-** Sleep Method, Power gating, Sleepy stack, Sleep, Stack, Zigzag, Dual sleep, Dual stack , MTCMOS, Fine-grain power gating, coarse-grain power gating.

I. INTRODUCTION:

The process of scaling technologies to nano-meter regime has resulted in a rapid increase in leakage power dissipation (static and dynamic power dissipation). Reduce the static power dissipation has become extremely important during periods of inactivity to develop design techniques. Without trading-off performance the power reduction must be achieved which makes it harder to reduce leakage during (normal) operation at runtime .In sleep or standby mode to reduce the leakage power there are several techniques are used. Well known technique is Power gating technique where a sleep transistor is added between virtual ground (circuit ground) & actual ground rail. In the sleep mode to cut-off the leakage path, the device is turned-off. This technique provides a substantial reduction in leakage at a minimal impact on performance. It has been shown that the Power Gating technique uses high Vt sleep transistors. When the block is not switching high sleep transistors are cut off VDD from a circuit block. An important design parameter is size of the sleep transistor this technique also known as MTCMOS (Multi-Threshold CMOS).

To achieve long term leakage power reduction an externally switched power supply is a very basic form of power gating. Internal power gating is more suitable to shut off the block for small intervals of time. Power can be controlled by power gating controllers and to provide power to the circuitry CMOS switches are used.The power gated outputs block discharges slowly. Hence voltage levels of the output block spend more time in threshold voltage level (Vth), so it leads to larger short circuit current in the circuit.

Low-leakage PMOS transistors are used as header switches to shut off power supplies , the Power Gating parts of a design in the mode of sleep or standby. NMOS footer switches can also be used as sleep transistors in the design of power gating technique. The sleep transistors can be inserting to splits the chip's power network into a permanent power network connected to the power supply and a virtual power network that drives the cells and can be turned off. By using of cell- or cluster-based (or fine grain) approaches or a distributed coarse-grained approachs Power Gating can be implemented.

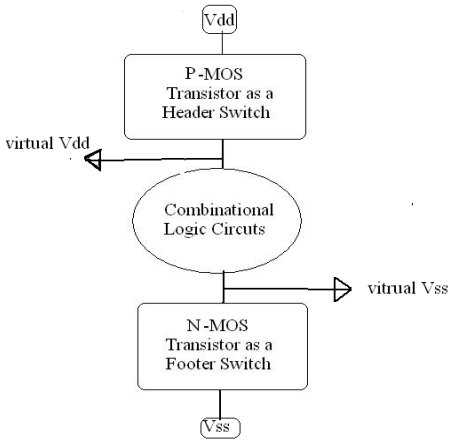

Fig1: Power Gated Circuits

II. Power-Gating (PG) Parameters

For a successful implementation of this methodology the following parameters are need to be considered and their values must be carefully choose.

1. **Size of the Power Gate:** The size of the power gate must be selected to handle the amount of switching current at any point of given time. The gate must be bigger such that there is no measurable voltage (IR) drop due to the gate. The size of the gate is selected to be around 3 times of the switching capacitance because as a Rule of Thumb.

   The Designers can also choose header (P-MOS) or footer (N-MOS) gate for the designing circuits. For the same switching current N-MOS footer gates are to be smaller in area. Switching current can be accurately measured by using of Dynamic power analysis tools & can predict the size for the PG

2. **Slew rate:** To determine the power gating efficiency it is an important parameter in power gating. It takes more time to switch off and switch-on the circuit, when the slew rate is large & hence it is affects on the power gating efficiency also. The gate control signal is used to control the slew rate

3. **Switching Capacitance:** This important constraint refers to that without affecting the power network integrity the amount of circuit can be switched simultaneously. If a large amount of the circuit is switched simultaneously, the resulting "rush current" can compromise the power network integrity. The circuit needs to be switched in stages in order to prevent this.

4. **Leakage of Power Gate:** by using of active transistors power gates are designed, to maximize power savings the leakage reduction is an important consideration.

i) Fine Grain Power Gating(FGPG)

Sleep transistor is added to every cell that is to be turned off imposes a large area penalty & individually gating the power of every cluster of cells creates timing issues introduced by inter-cluster voltage variation, these are very difficult to resolve. FGPG encapsulates the switching transistor as a part of the standard cell logic in the design.The library IP vendor or standard cell designer are used to design the Switching transistors.Usually these cell designs can easily be handled by EDA tools for implementation & conform to the normal standard cell rules.

The gate control size is designed considering the worst case scenario, it will require the circuit to switch during every clock cycle, in a huge area impact on result only for the low Vt cells Some of the recent designs implement the FGPG selectively.If the multiple Vt libraries are allows by the technology then.In the design the use of low Vt devices (20%) is minimum, so area can be reduced.

If the next stage is a high Vt cell then the output must be isolated on the low Vt cells by using of PG'S.When output goes to an unknown state due to power gating, it can be cause the neighboring high Vt cell to have leakage.For the control signals, Slew rate of Gate control constraint is achieved by having a buffer distribution tree. Buffers without the gate control signal designed with high Vt cells (The buffers must be chosen from a set of always on buffers). When a cell switches off with respect to another, it minimizes the rush current during switch-off & switch-on.Usually the high Vt device is designed as a gating transistor.

CGPG offers further flexibility by optimizing the PG cells where there is low switching activity in the design.At the CG level Leakage optimization had to be done , changing the high leakage cell for the low leakage one.FGPG is a methodology resulting in leakage reduction up to 10 times. If the power reduction requirement is not satisfied by multiple Vt optimization, this type of power reduction makes it an appealing technique.

ii) Coarse-Grain Power Gating(CGPG)

The CGPG Process implements the grid style sleep transistors which drives cells locally through shared virtual power networks.This technique is less IR-drop variation, introduces less sensitive to PVT variation & imposes a smaller area overhead than the implementations based on cell- or cluster.In CGPG, the PG transistor is a part of the power distribution network rather than the standard cell. Implementation of a CG structure is in two ways those are

1. **Based on Ring:** The power gates are placed around the perimeter of the module that is being switched-off as a Ring. To turn the power signals around the corners by using of special corner cells

2. **Based on Column:** Within the module the power gates are inserted with the cells abutted to each other in the form of columns.The switched power is in the lower layers, while the global power is the higher layers of metal.

At any given time, overall switching current of the module depends on the Gate sizing. Since only a fraction of circuits switch at any point of time, FG switches are larger as compared to the Power Gate sizes.By using of worst case vectors can determine the worst case switching for the module and the size in dynamic power simulation. In the analysis the IR drop can also be factored. A major consideration in CGPG implementation is Simultaneous switching capacitance. By the simultaneous switching special counters can be used to selectively turn on blocks of switches & in order to limit simultaneous switching, gate control buffers can be daisy chained.

III PREVIOUS METHODS

The problem of controlling/optimizing the power gating parameters can be solved by clustering based approach. In the power mode transitions the important design considerations are minimizing the total size of sleep transistors, the peak current, and the wakeup delay.
This work solved the problem of finding logic clusters, analyzes the relations between the three parameters, performance loss constraints and that minimize the wakeup delay (wakeup schedule)while satisfying the peak current.

To reduce the leakage power there are so many techniques are existed. Sleep transistor should be in ON, if we are working with the logic circuits. A variation of the Sleep Technique , the zigzag Technique, reduces wake- up overhead caused by sleep transistors.By placement of alternating sleep transistors assuming a particular pre-selected input vector [6]. Another technique is the stack technique for leakage power reduction, by breaking down an existing transistor into two half size transistors [7]. Then these half size transistors increase delay & could limit the usefulness of the technique

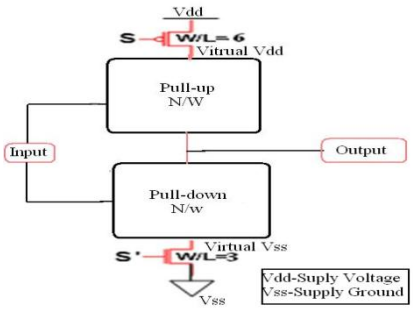

Fig2: Sleep Technique

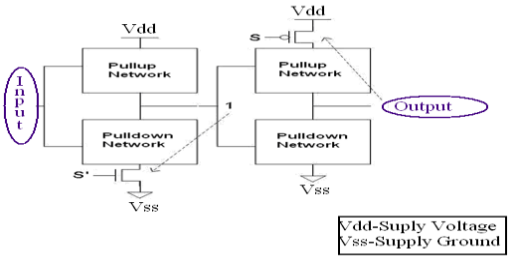

Fig3: Zigzag Technique

The Sleepy Stack Technique (Fig. 4) combines the Stack & Sleep techniques [2, 3]. The existing transistors divided into two half size transistors in the Sleepy Stack technique like as Stack technique. Between the divide transistors one of sleep transistor will be added in parallel. Stacked transistors suppress leakage current while saving state & Sleep transistors are turned off during sleep mode.
In active mode it reduces delay & resistance of the path because of sleep transistor, sleep transistor is placed in parallel to the one of the stacked transistors

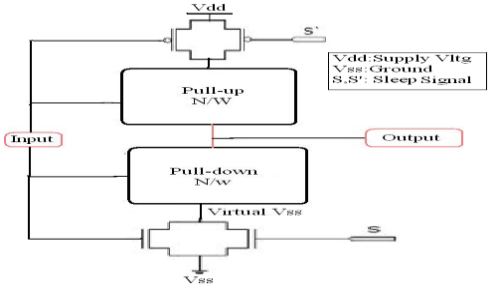

Fig4: Sleepy Stack Technique

However, area requirement is maximum for this technique since every transistor is replaced by three transistors.Dual sleep Technique[8] is (Fig:5) uses the advantage of using the two extra pull- up & pull-down transistors in sleep mode either in OFF/ON state. To all logic circuitry the dual sleep portion is designed as common. For a certain logic circuit less number of transistors are enough to apply

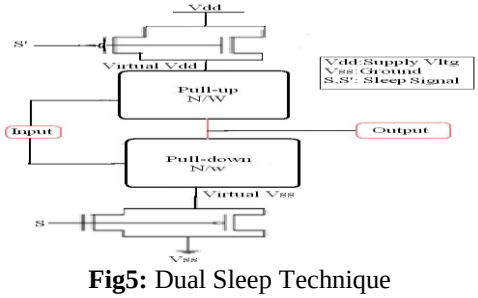

Fig5: Dual Sleep Technique

The method is dual stack approach [1], in sleep mode, the sleep transistors are off, i.e. transistor N1 andP1 are off. We do so by making S=0 and hence S'=1. Now we see that the other 4 transistors P2, P3 and N2, N3 connect the main circuit with power rail. Here we use 2 PMOS in the pull down network and 2 NMOS in the pull-up network. The advantage is that NMOS degrades the high logic level while PMOS degrades the low logic level. Due to the body effect, they further decrease the voltage level. So, the pass transistors decreases the voltage applied across the main circuit.

As we know that static power is proportional to the voltage applied, with the reduced voltage the power decreases but we get the advantage of state retention. Another advantage is got during off mode if we increase the threshold voltage of N2, N3 and P2, P3. The transistors are held in reverse body bias. As a result their threshold is high. High threshold voltage causes low leakage current and hence low leakage power. If we use minimum size transistors, i.e. aspect ratio of 1, we again get low leakage power due to low leakage current. As a result of stacking, P2 and N2 have less drain voltage. So, the DIBL effect is less for them and they cause high barrier for leakage current. While in active mode i.e. S=1 and S'=0, both the sleep transistors (N1 and P1) and the parallel transistors (N2, N3 and P2, P3) are on. They work as transmission gate and the power connection is again established in uncorrupted way. Further they decrease the dynamic power.

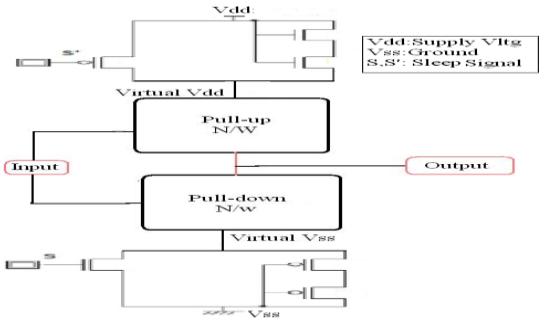

Fig6: Dual Stack Technique

IV. PROPOSED METHOD

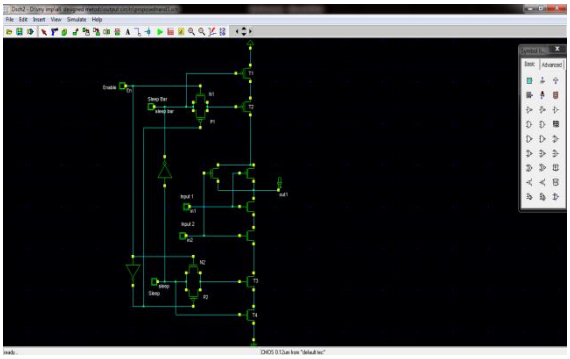

Fig7: Power Gated Sleep Method Technique

In the Proposed method there are three modes of operations

(i) In Active mode (AM)
(ii) In Standby mode (SM)
(iii) Sleep to Active mode transition (SAM)

In AM, both the N2 & P2 sleep transistors remain ON & the sleep Signal (S) of the transistor is held at logic'1' (high). In this case virtual Vss node potential is pulled down to the ground potential, making the logic difference between the logic circuitry approximately equal to the Vdd (supply voltage) & both transistors offer very low resistance. To combining stacked sleep transistors, the magnitude of power supply fluctuations will be reduced because these transitions are gradual during sleep mode transitions, a stacked sleep structures can achieve

minimum leakage the with a normal threshold device, while conventional power gating uses a sleep transistor which is a high- threshold device to minimize leakage[2].

In SM, both the T3 & T4 sleep transistors remain ON & the sleep Signal of the transistor is held at logic'1' (high) & control transistors P2 & N2 is OFF by giving logic'0, In this case virtual Vss node potential is pulled down to the ground potential, making the logic difference between the logic circuitry approximately equal to the Vdd (supply voltage) & both transistors offer very low resistance By using of the stacking effect we can reduces the leakage current, turning both sleep transistors OFF(T3 & T4) and vice-versa for the header switch.

In SAM, the analyzed design gives major contribution in terms of peak of SM compared to stacking PG. when Sleep mode occurred, the circuit is going from sleep to active or active to sleep. In initial stage, by turning on the control transistor M1 (which is connected across the drain and gate of the T3) then the sleep transistor (T3) is working as a diode.

Due to this Ids of the sleep transistor T3 drops in a quadratic manner. This reduces the circuit wake-up time, voltage fluctuation on the power net & ground.So in SAM, initially after small duration of time we are turning ON transistor T3, to reduce the Ground Bounce Noise T4 will be turned ON. In next stage control transistor is off that sleep transistor works normally. During sleep to active mode transition, transistor T3 & T4 (after a small duration of time) is turned ON. The logic circuit isolated from the ground for a short duration as the transistor T4 is turned OFF. During this duration, the transistor T4 is operated in triode region, by controlling the intermediate node voltage we can reduce the Ground Bounce Noise & Inserting proper amount of delay (delay < discharging time of the T3transistor). By turning both T3 andT4 sleep transistors OFF, the Leakage current is reduced by the stacking effect. Due to small Id (drain current) it raises the intermediate node voltage VGND2 to +ve values

+ve potential at the intermediate node has 4 effects

- Vgs of T3 becomes negative.
- Negative (body-to-source potential) Vdsl of T3decreases, resulting in less drain induced barrier lowering
- Vds of T4 is less compared to T3, because most of the voltage drops across the T3 in sleep mode.
-

This significantly reduces the drain barrier lowering. Hence the reduction of leakage power is done in circuit [7].

V. SIMULATION RESULT

Fig7 & Fig8 show the logic and power consumption, respectively for an NAND. For circuit design & circuit logic verification we use DSCH (Digital schematic), for CMOS layout verification & power calculation of the circuit we use MWND(Microwind) Fig7 & Fig8 show the logic and power consumption, respectively for an NAND

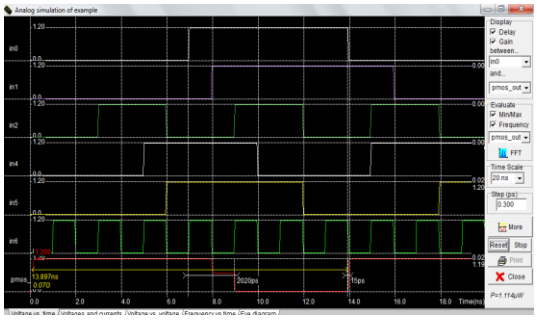

Fig8: Power consumption of proposed technique

Circuit Technique	Power Consumption
Sleepy NAND	1.844 µW
Dual Sleep NAND	1.785 µW
Proposed NAND	1.114 µW

Table 1: Comparison b/w Proposed method with other techniques

VI.CONCLUSION

Sub threshold leakage power consumption is a great challenge in nano-meter scale (CMOS) technology, although previous techniques are effective in some ways, no perfect solution for reducing leakage power consumption is yet known. Therefore, based upon technology & design criteria the designers can choose the techniques. In this paper, we provide novel circuit structure in terms of static & dynamic powers named as "Power gated sleep method" it's a new remedy for designers. This technique shows the least speed power product among all techniques. The Proposed technique achieving ultra-low leakage power consumption with much less speed, especially it shows nearly 50-60% of power than the existing. So, it can be used for future IC'S for area & power Efficiency

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