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Reduced Switch Single-Phase Five-Level Inverter for Grid Connected PV System

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Abstract: A reduced switch multi-level inverter for grid connected photovoltaic (PV)system is presented in this paper. A conventional grid connected PV system uses full-bridge inverters which results a three level output. Inverter output THD can be reduced by increasing its number of levels. For that we can use conventional multi-level inverters like diode clamped, flying capacitor and cascaded-H bridge. But, in all these topologies, the number of circuit elements increases with increase in number of levels. The multi-level inverter discussed in this work offers higher power capability with lower harmonics and lower switching losses with an additional advantage of reduction in the number of power electronic switches using an auxiliary circuit arrangement. A conventional grid PV system and PV system with reduced switch five-level inverter are simulated using MATLAB/Simulink and the results are analyzed. Also, in simulation THD of the above two systems are compared.

Keywords: Five level inverter, Grid connected PV System, Multi-level inverter, P&O MPPT algorithm, Reduced switch multi-level inverter, Renewable energy.

1. Introduction

Because of the rapid population growth and industrialization, the demand for electricity is growing day by day, and we may not be able to meet our demands with our central power generation system. Also the diminishing deposits of non-renewable energy sources such as coal, natural gas, fossil fuels etc. leads to energy crisis. So new technologies should be developed to produce energy in a most environment-friendly manner and it should be utilized in a most efficient way. We have to find use of other sources like solar, wind, geothermal etc. for energy generation other than our conventional sources like hydro, thermal and nuclear. Out of these renewable sources, one of the main sources is solar energy.

Solar energy is a renewable, inexhaustible and ultimate source of energy and the photovoltaic technique which uses solar energy has its own advantages like the source is quite free, no fuel is required, produces no waste etc.However, PV system has gained less support from private sectors and users due to the high cost to install the system and long payback time from the system.

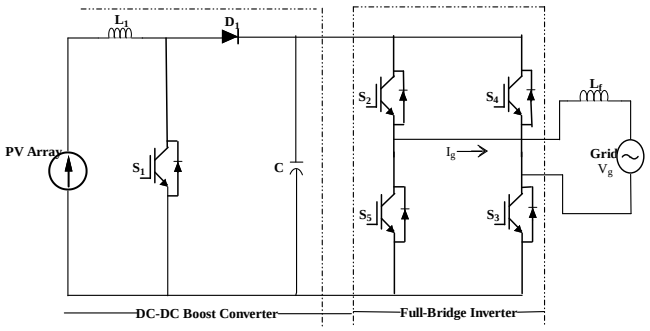

Fig.1 Conventional grid connected PV system

A conventional single phase photovoltaic system which is shown in Fig.1 comprises a boost converter and an inverter .The output of PV array is stepped up using dc-dc converter (either boost or buck-boost can be used) and after inversion it is fed to grid/load.

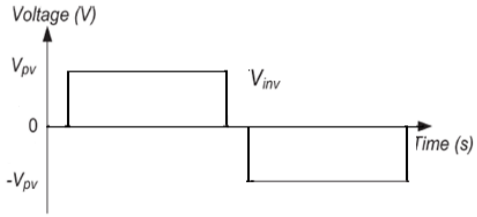

Fig.2 Output voltage levels of a full bridge inverter with V_{pv} as input

In conventional system, we are using a full bridge inverter which results a three level output, ie +voltage, zero and –voltage levels. Ideal three-level output of an inverter is shown in Fig.2. If we need more sinusoidal output from the inverter or if we want to reduce the THD of inverter output, we can increase the number of levels of the inverter. For that we can use multi-level inverters. The conventional multi-level topologies are diode clamped, flying capacitor and cascaded-H bridge. But the main problem with these multi-level inverters are, if we increase the number of levels, the number of switching devices and other circuit components have to be increased. Thus the system size increases, cost increases, circuit complexity increases and the control will become more difficult.

2. Grid Connected Pv System With Reduced Switch Five-Level Inverter

A single-phase grid connected PV system with reduced switch five-level inverter is shown in Fig.3 [6] and [7]. The inverter adopts a full-bridge configuration with an auxiliary circuit. PV arrays are connected to the inverter via a dc–dc boost converter to step up the output of PV module.By introducing an auxiliary circuit between dc-dc converter and full-bridge inverter, we can increase the number ofinverter output levels to five which is shown in Fig.4 [5].

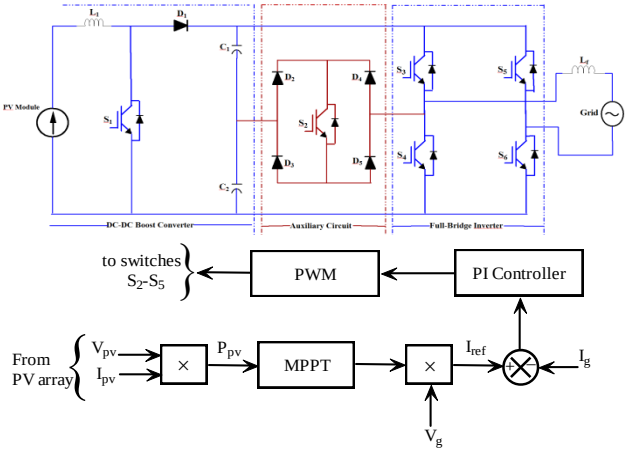

Fig.3 Grid connected PV system with reduced switch Five-level inverter

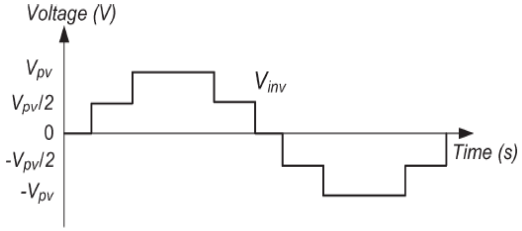

Fig.4 Output voltage levels of a five-level inverter with V_{pv} as input

The auxiliary circuit consists of one switch and four diodes. So here a total of five switches, ie one switch of this auxiliary circuit and four switches of full bridge inverters are enough to get a five-level output. But, all other conventional multi-level inverters require a minimum of eight power electronic switches to generate a five-level output. Thus the system cost reduces, size reduces and circuit complexity reduces.

A filtering inductance L_f is used to filter the current injected into the grid. The injected current must be sinusoidal with low harmonic distortion. PI current control scheme is employed to keep the output current sinusoidal and to maintain the power factor at near unity. The irradiance level in inconsistent throughout the day, the amount of electric power generated by this solar module is changing with weather conditions. To overcome this problem or to track the maximum power from solar array, maximum power point tracking (MPPT) algorithm is used. The feedback PI current control senses the current injected into the grid, also known as grid current I_g and feedback to a comparator which compares it with the current I_{ref}. I_{ref} is obtained from the grid voltage by multiplying it with the variable m. Variable m is derived from the MPPT algorithm. As the irradiance level increases, m also increases and we can represent it as 'm' α irradiance of the sun

The instantaneous current error from the comparison between I_{ref} and I_g is fed to a PI controller. The integral term of PI controller improves the tracking by reducing the instantaneous error between the reference and the actual current. The resulting error signal is compared with a triangular carrier signal and the control signals for full bridge inverter are generated based on this comparison. This is to ensure that grid current is in phase with grid voltage and always at near unity power factor.

a. Working Principle-(Dual Reference Modulation Technique)

Two reference signals V_{ref1} and V_{ref2} will take turns to be compared with the carrier signal at a time [6] and [7]. If V_{ref1} exceeds the peak amplitude of the carrier signal $V_{carrier}$, V_{ref2} will be compared with the carrier signal until it reaches zero. At this point onward, V_{ref1} takes over the comparison process until it exceeds $V_{carrier}$. This will lead pattern, as shown in Fig.5. Switches S_2–S_4 will be switching at the rate of the carrier to a switching signal frequency, whereas S_5 and S_6 will operate at a frequency equivalent to the fundamental frequency.

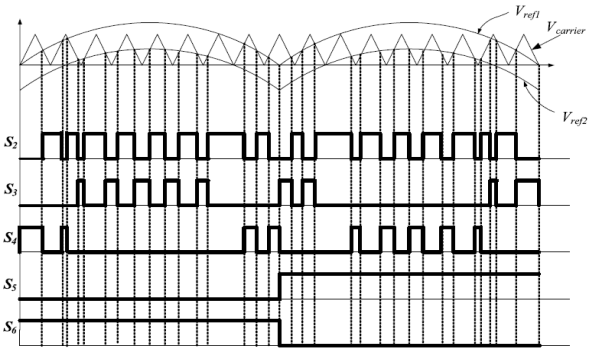

Fig.5 Switching pattern for the single phase five level inverter

b. Power Stage Operation

The required five voltage output levels (V_{dc}, $V_{dc}/2$, 0, $-V_{dc}/2$, $-V_{dc}$) are generated as follows:

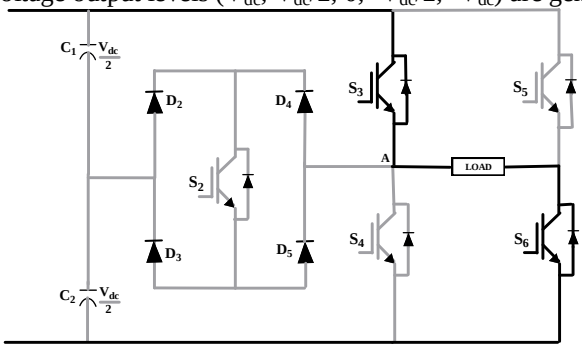

Fig.6 Switching pattern required to generate output voltage level V_{dc}

1) Maximum positive output, V_{dc}: Switch S_3 is ON, connecting the load positive terminal to A, and switch S_6 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF. Fig.6 shows the current paths that are active at this stage.

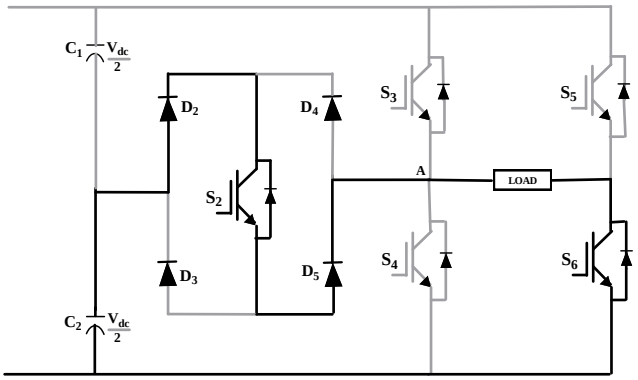

Fig.7 Switching pattern required to generate output voltage level $V_{dc}/2$

2) Half-level positive output, $V_{dc}/2$: The auxiliary switch, S_2 is ON, connecting the load positive terminal to point A, through diodes D_2 and D_5, and switch S_6 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF. Fig.7 shows the current paths that are active at this stage.

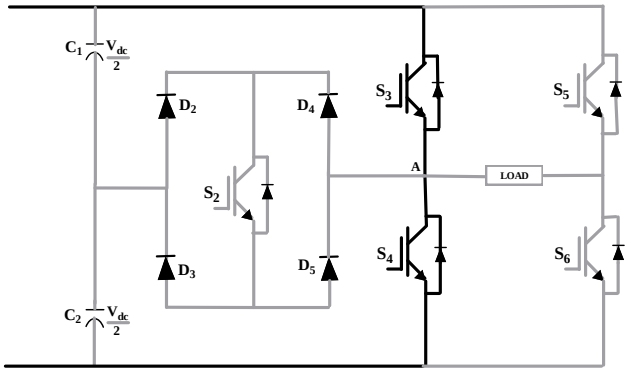

Fig.8 Switching pattern required to generate output voltage level zero.

3) Zero output: The two main switches S_3 and S_4 are ON, leads to short-circuit. All other controlled switches are OFF. Fig.8 shows the current paths that are active at this stage.

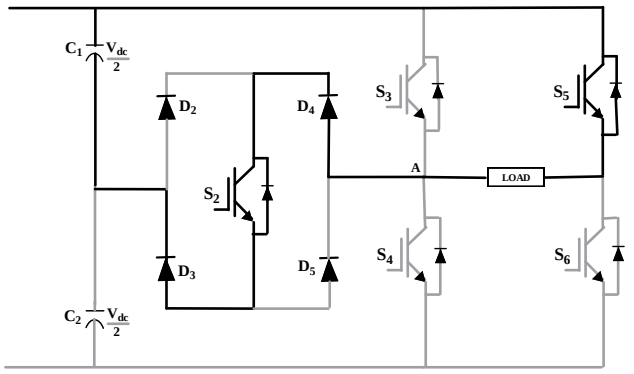

Fig.9 Switching pattern required to generate output voltage level $-V_{dc}/2$

4) Half-level negative output, $-V_{dc}/2$: The auxiliary switch, S_2 is ON, connecting the load positive terminal to point A, through diodes D_3 and D_4, and S_5 is ON, connecting the load negative terminal to ground . All other controlled switches are OFF. Fig.9 shows the current paths that are active at this stage.

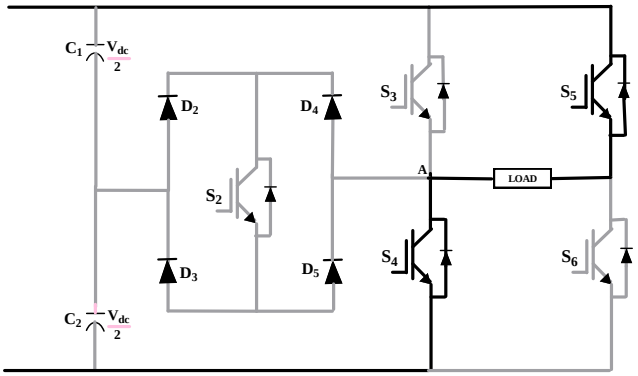

Fig.10 Switching pattern required to generate output voltage level $-V_{dc}$

5) Maximum negative output, $-V_{dc}$: Switch S_5 is ON, connecting the load negative terminal to A, and S_4 is ON, connecting the load positive terminal to ground. All other controlled switches are OFF. Fig.10 shows the current paths that are active at this stage.

Table I gives the switching combinations to generate the five-level output with reduced switch topology and Table II gives the comparison of different multi-level inverter topologies on the basis of number of circuit components to get a five-level output

Table I : Switching combinations to generate five level output

S_2	S_3	S_4	S_5	S_6	V_{out}
ON	OFF	OFF	OFF	ON	$+V_{dc/2}$
OFF	ON	OFF	OFF	ON	$+V_{dc}$
OFF	OFF or (ON)	OFF or (ON)	ON or (OFF)	ON or (OFF)	0
ON	OFF	OFF	ON	OFF	$-V_{dc/2}$
OFF	OFF	ON	ON	OFF	$-V_{dc}$

Table II : Comparison of different multi-level inverter topologies

Converter type:	Diode clamped	Flying capacitor	Cascaded H-Bridge	Reduced switch
Switching devices	8	8	8	5
Main diodes	8	8	8	8
Clamping diodes	6 or 12	0	0	0
Capacitors	4	5	2	2

2.3 MPPT for PV system

The output of PV panel changes with the changes in climatic condition such as temperature and insolation level. In order to track maximum power from solar array, maximum power point trackers (MPPT) are used. P-V and I-V characteristic of a PV module with maximum power point (MPP) is shown in Fig.11.

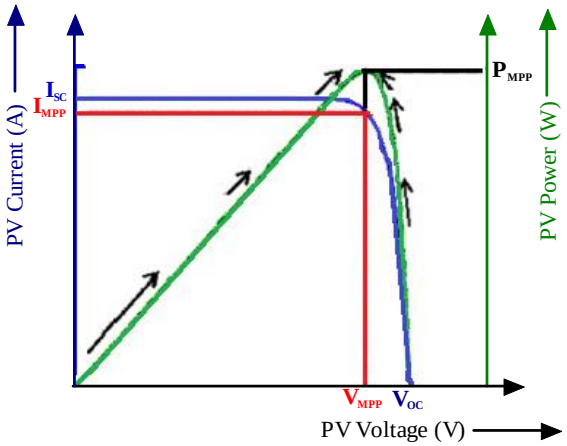

Fig.11 P-V and I-V characteristics of a PV module

Many MPPT techniques have been developed for PV systems to track the maximum power point of the system; examples are the Perturb and Observe (P&O), Incremental Conductance (IC), MPPT based on FLC etc. The P&O algorithm is very popular and simple. This method finds the maximum power point of PV modules by means of iteratively perturbing, observing and comparing the power generated by the PV modules. It is widely applied to the maximum power point tracker of the photovoltaic system for its features of simplicity and convenience. The required parameters for P&O MPPT algorithms are only the voltage and current of PV module.

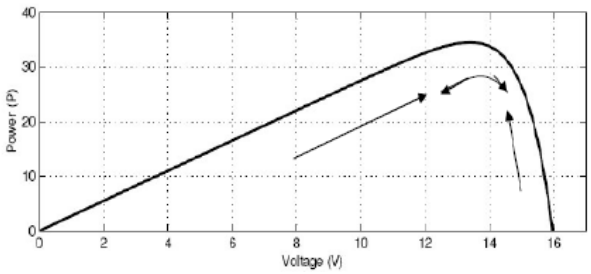

Fig.12 Power graph for P&O algorithm

The power graph of PV system is shown in Fig.12. In P&O algorithm a slight perturbation (ΔD=0.01) is introduced in the system. This perturbation causes the power of the solar module to change. If the power increases due to the perturbation, then the perturbation is continued (D+ ΔD) in that direction. After the peak power is reached, the power at the next instant decreases and hence after that the perturbation reverses (D- ΔD). The flow chart of P&O MPPT algorithm is shown in Fig.13

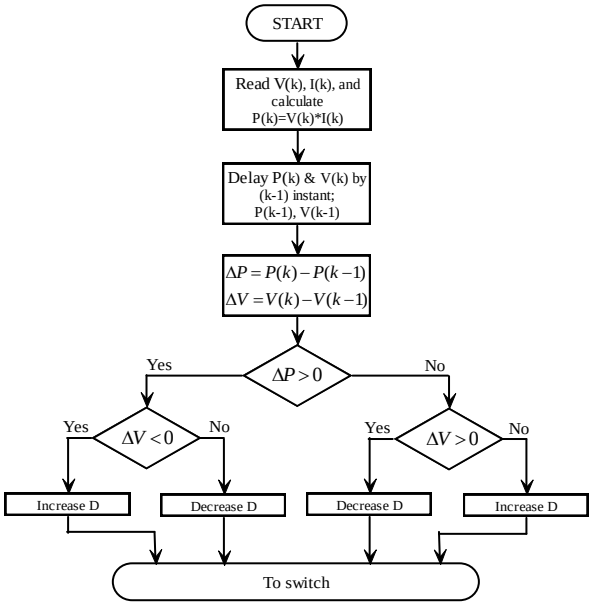

Fig.13 Flow Chart of P&O MPPT Algorithm

3. Simulation Results

Fig.14 (a) and Fig.14 (b) gives the P-V and I-V characteristics of PV array at constant temperature and for varying irradiance respectively.

Irradiance:

I-1000W/m^2 II-900W/m^2
III-800W/m^2 IV-500W/m^2

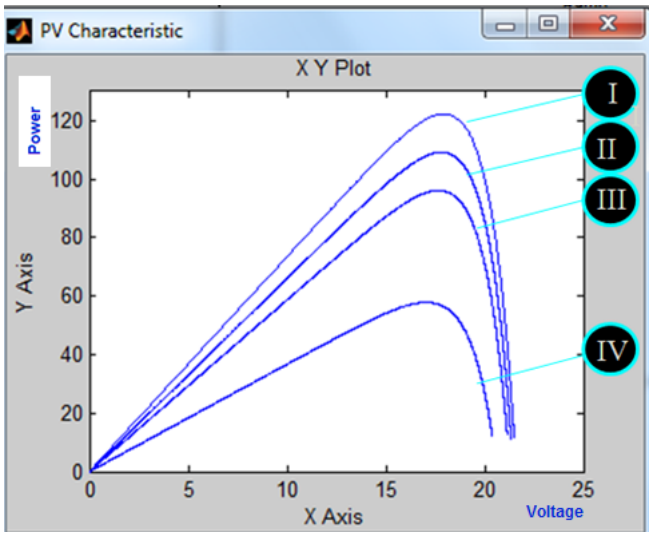

Fig.14 (a) PV characteristic of PV array at constant temperature and for varying irradiance

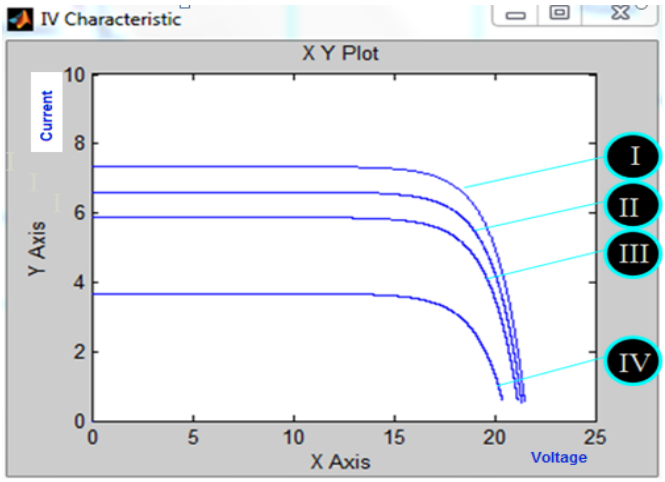

Fig.14 (b) IV characteristic of PV array at constant temperature and for varying irradiance

The two reference signals and the carrier signal for dual reference modulation PWM technique are shown in Fig.15 and the control signals to switches S_2-S_6 are shown in Fig.15 (a) to Fig.15 (e).

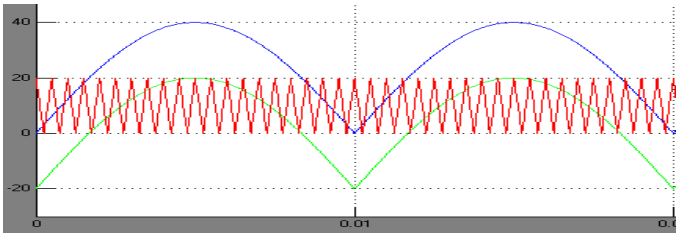

Fig.15 PWM signal generation (Dual reference modulation)

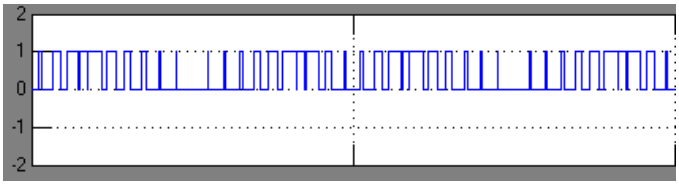

Fig.15 (a) PWM switching signal to S_2

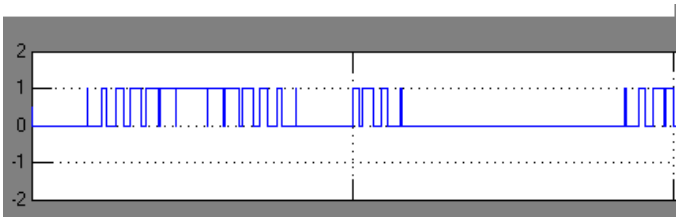

Fig.15 (b) PWM switching signal to S_3

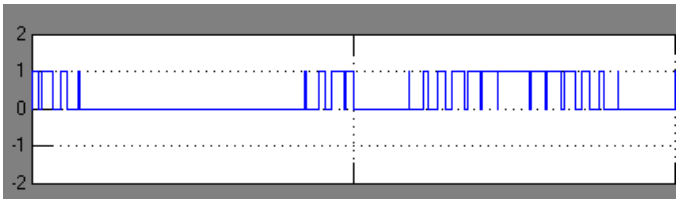

Fig.15 (c) PWM switching signal to S_4

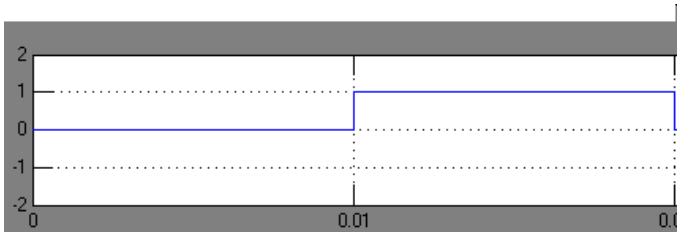

Fig.15 (d) PWM switching signal to S_5

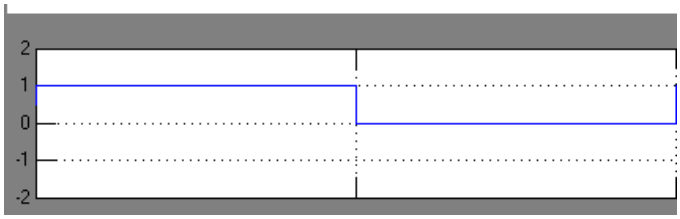

Fig.15 (e) PWM switching signal to S_6

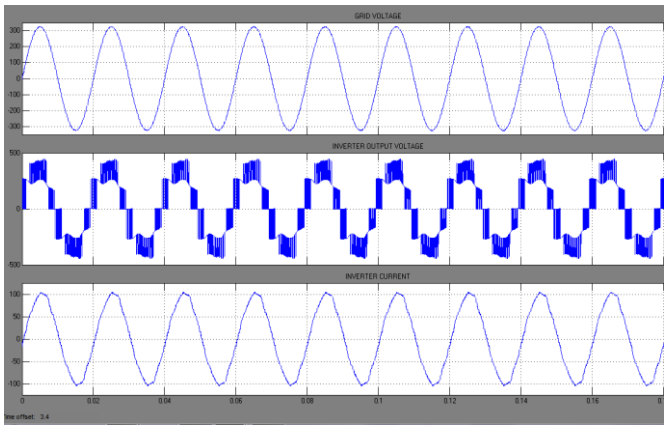

Fig.16 Grid voltage, inverter output voltage and inverter current of PV system with reduced switch topology

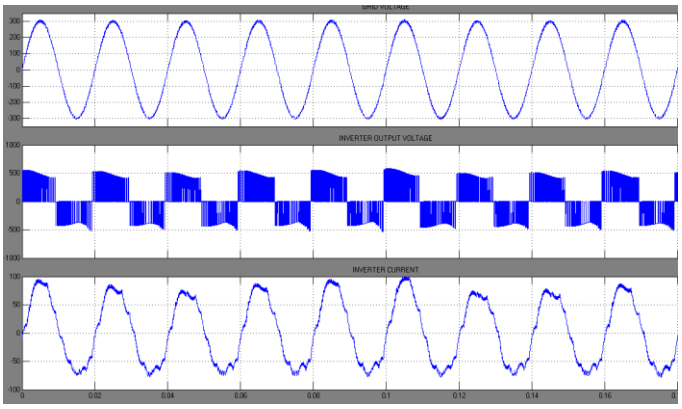

Fig.17 Grid voltage, inverter output voltage and inverter current of conventional PV system

Grid voltage, inverter output voltage and inverter current of PV system with reduced switch topology and conventional PV system are given in Fig.16 and Fig.17 respectively.

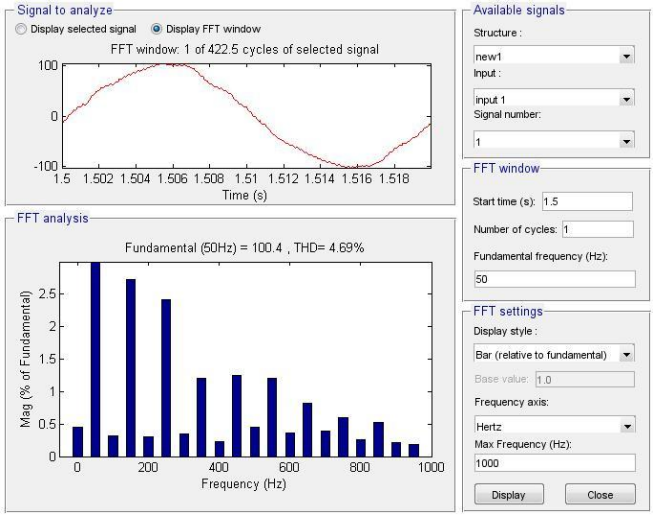

Fig.18 (a) FFT analysis for PV system with new topology

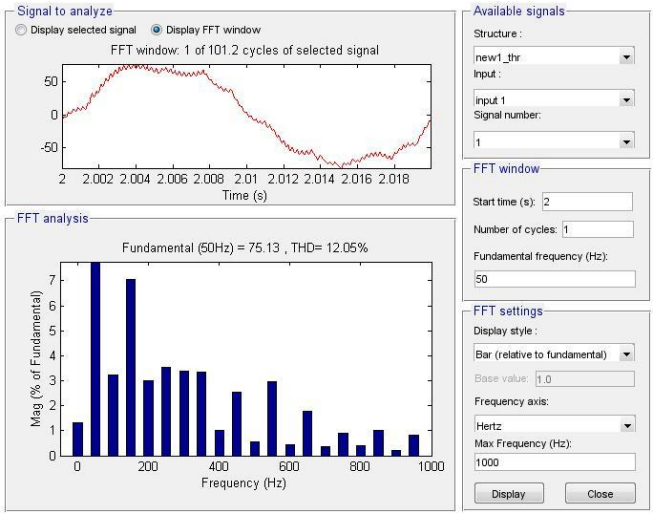

Fig.18 (b) FFT analysis for Conventional PV system

From FFT analysis shown in Fig.18 (a) and Fig.18 (b)it is very clear that THD can be reduced with an auxiliary circuit arrangement between boost converter and full bridge inverter compared to conventional PV system.

4. Conclusions

In this paper, a single phase photovoltaic system with reduced switch five-level inverter is presented. The circuit topology, control algorithm and operational principle of this inverter are analyzed in detail. To generate a five-level output, this new topology requires lesser number of power electronic switches and other circuit elements compared to conventional multi-level topologies. So the system cost can be reduced, circuit complexity can be reduced.A conventional PV system and PV system based on reduced switch multi-level inverter are simulated using MATLAB/SIMULINK and are compared on the basis of power quality and total switching losses. And the simulation results prove that with this new topology THD can be reduced. In this new topology lesser number of switches are switching at high frequency compared to conventional system, so the total switching losses can be reduced.

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