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Structural design of Mixed Signal IP block

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Abstract: In VLSI domain as technology is scaling down, physical design is becoming green computing topic in electronic design automation. Physical design plays significant role in improving frequency and power computation. In any VLSI physical design flow, along with area, power and delay there is tradeoff between turnaround times. Physical design automation can help in improving turnaround time factor along with quality of final product. In any VLSI design it is mandatory that design must operate correctly at desired clock frequency. Along with timing it is always good to have chip with lower area and minimum power consumption. Before tape out it is assumed that design is free from all errors and warnings and is optimized in best possible way. Some automation has been done in order to get optimal and accurate result with given constraints. As success of any product highly depends on performance of chip and time to market automation helps to improve both of these factors. This paper cover efforts done to make error free design for mixed signal IP block.
Keywords: Structural design, Physical design, Synthesis.

I. INTRODUCTION

Very Large Scale Integration (VLSI) is a field where technology is changing every year. Each day comes up with new challenges. As per Moore's law, density of transistor on chip gets multiplied by two every eighteen months. As technology is scaling down day by day this laws appears to be unrealistic. In order to maintain quality of product modern fabrication technologies and design automation tools facilitates industry to follow Moor's law. Shrinking of technology implies reduction of gate length, which in turn increases complexity of design. Now a days, demand of more functionality in single chip with same area results in increase in complexity of the design. Because of unavailability area parasitic elements such as resistance and capacitance starts dominating. Sometimes there is possibility that this complexity of design may cost in quality and efficiency of design.

To combat these challenges, industry restores automation in various phases of design. It is unthinkable to design VLSI product without use of any automation technique. These automation tools takes care of every aspect of design. Minimum area, fast operating speed and minimum power consumption are the feature of good chip. But, practically it is very difficult to achieve all three. These automation tool helps us to optimize VLSI chip design in best possible way.

In any industry, time to market of a product and performance of product determines its success. In VLSI industry it is compulsory to check timing closure, performance, power requirement, design rules, LVS etc. before tape out of design. For checking all these parameters designer has to spend substantial efforts. Out of all these timing closure has highest priority. Because of tight area constraints, power budget as well as reliability issue it is not possible to get timing clean reports in single iteration. It is very difficult to fix all these issues manually. Using automation it is possible to fix more than one violation in single iteration. And hence due to complexity and repetitive methods of fixing violations it is possible to automate timing closure. So timing closure is one area where lot of automation is done and still has lot of scope for further automation.

As technology is scaling down and because of demand of high operating frequency, parasitic are becoming significant. In submicron technology, it is must to consider interconnect parasitic because this can have significant impact on timing performance. This makes timing closure more challenging. Also along with these parasitic noise is also becoming significant. Because of these interconnect and tight constraints last optimization is becoming critical.

II. METHODOLOGY AND SOLUTION

A. Physical design

Day by day design complexity is increases because of shrinking of technology and increase in number of transistor. Because of increase in complexity larger chip is divided smaller parts commonly known as blocks. This block level implementation is known as hierarchical design. This hierarchical design procedure makes designing process simpler to some extent. But, complexity due to routing of signal interconnecting two block may increase.

Basic VLSI design flow is divided into two parts. One is front end design other is backend. Depending on specifications given by user system level algorithm is designed and this algorithm is used to generate RTL (register transfer level) code. This process of generating RTL description comes under front end design. After completion of front end design physical placement of cells on chip and connecting those cells with net most commonly known as routing comes under backend. These various steps from synthesis to sign off (tape out) comes under backend design. Backend design flow consists of various steps. Two main phases of design are generation of net list from RTL and second step is from net list to production worthy layout. Basic block diagram of backend design flow is shown in figure 1.

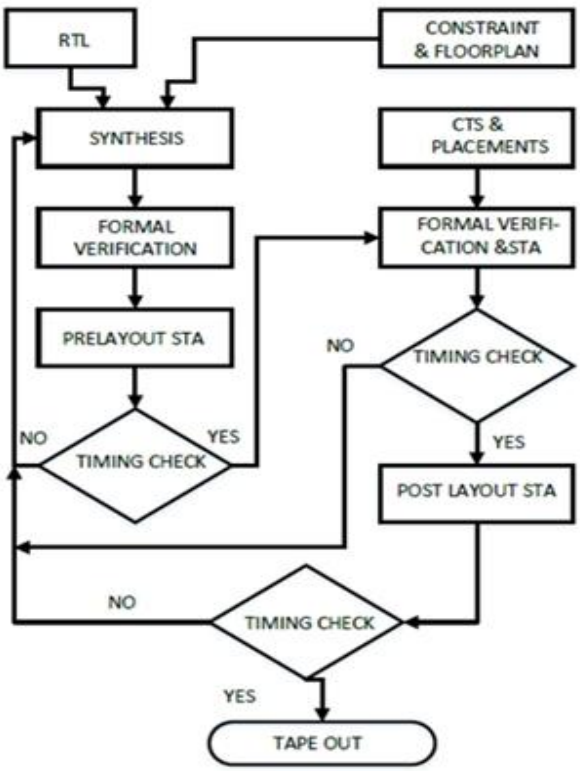

Figure 1: Physical design flowchart

B. Synthesis

Synthesis is the first step of any backend flow. Main purpose of this synthesis is to get gate level net list from RTL.

C. Formal Verification

Second step in flow is formal verification. Formality verification can be performed between RTL versus RTL and net list versus RTL and net list versus net list. There are three phases of verification read phase

match phase and verification phase. In general as per names in first step tool reads all .v or .db. Files. In second phase comparison between generated and golden reference is performed and report of comparison is generated in third phase. Formal verification is performed in order to ensure functionality of design. The ultimate goal of formal verification is to ensure that net list and RTL has same functionality. This verification can be performed hierarchically in order to reduce complexity. As this approach allows to divide design into small parts and perform formal verification on each part simultaneously which reduces complexity as well as time required. This approach is called as divide and conquers. Entire design is divided into small parts and these smaller parts including interfacing pins are mapped into RTL these sub designs are known as cones. In order to ensure proper check design must have sufficient number of mapping points. These mapping points are nothing but outputs of sequential pins. Large number of mapping points reduces probability of missing of unmatched points.

D. Pre-layout STA

In VLSI design flow process timing analysis is performed at various stages. In pre-layout simulation timing analysis is performed based on net list. Since in pre-layout simulation actual placement and routing information is not available and hence wire load models are used in order to calculate delay. Depending on area particular wire load model is selected which gives parasitic information. In pre-layout simulation tool place cells and performs temporary routing in order to obtain timing information of the design. Pre-layout STA does not give exact scenario of timing information but it will give approximate idea about timing in design.

E. Floorplan

In floor planning we estimate size of chip in short it gives area of design. Floor plan is physical representation of RTL description. Net list generated from synthesis is provided as input to floor plan tool. Net list contains macros, blocks and logic cells. In floor planning designer decides location of cells in net list, power grid, input output pins. While design floor planning area of chip play an important role in order to decide timing performance of design. As increase in area increases interconnect delay but it may cause problem while routing.

F. Placement

Process of deciding position of blocks on final chip area comes under placement. Based on cost reduction function of wire length, generation of hotspot, performance of chip, and creation of hotspot best position for particular cell or macro or block is decided. Placement is performed based on two algorithms one is iterative algorithm and other is constructive algorithm. In iterative improvement algorithm placement is performed again and again in order to get best possible solution for placement with minimum value of cost function. While, in constructive process placement is performed in global sense. Less congestion, small delay value, less number of metal layers comes under good placement.

G. Routing

Once placement is done next step is to connect those blocks with nets which comes under routing. Input to routing tool is placement information of cells and net list obtained from synthesis. While output of routing tool is complete connection of cells with nets. Routing is two-step process first step is global routing and second stage is detailed routing. Floor plan is applied as input to global routing. In global routing big routing problem is divided into smaller problems which are manageable. These smaller routings are performed in second stage that is detailed routing. Routing is always performed either in vertical or horizontal segments. These vertical and horizontal segments are connected using vias. Main objectives of routing are

- To reduce interconnect delay
- To reduce critical path delay
- To minimize wire length

Constraints to routing tools are maximum number of routing layers, DRCs, crosstalk and operating conditions.

H. Clock Tree Synthesis

Clock tree synthesis is a step where routing of clock net is performed. Initially from clock is distributed from single clock source but in such scenario it is very difficult to make clock available at every point at a same time. Reaching of clock at require point at same time is very important in order to ensure proper functionality of circuit. In order to make clock available at every point at a same time clock tree synthesis is performed. CTS

ensures that clock is distributed evenly to all gated elements and sequential cells. Also CTS guarantees less value of latency and skew at input of sequential elements. Though arrival of clock point at all elements simultaneously is ideal case, but CTS can ensure to achieve minimum variation using various clock distribution strategies. Two clock networks used in industry for clock distribution are clock mesh and clock tree.
There are various advantage and disadvantages of clock tree and clock mesh networks. Clock trees are used for ASICs having smaller size because of low routing requirement. Low routing length results in lower value of parasitic. But main disadvantage of clock tree routing is that, it is very difficult to balance the path delays because of asymmetrical placement of cells in design. And other disadvantage is these networks are very sensitive to variations. Tool usually uses simulated annealing algorithm in order to achieve best clock balanced tree network. There are different types of clock tree networks but H clock tree network is the most widely used one. H-type tree network is simplest one and is preferred for small structure. H-clock tree structure is shown in figure below

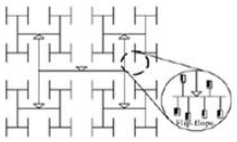

Figure 2.3: H-clock tree

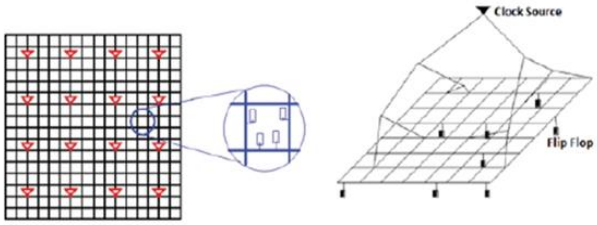

Figure 2: Clock mesh and H-tree global driver of clock mesh

For large design it is always better to use mesh distribution topology because it is always easy to use finite sets of buffers instead of using large number of sequential cell in order to reduce skew. Thus, mesh topology shows more robustness to variations and provides minimum clock skew. But the major disadvantage of mesh network is larger wire length which in turn results in increase in parasite, area power dissipation in network.

Various types of hybrid clock distribution technologies are available. Depending on application and complexity of ASIC particular network is selected for clock distribution. After routing of clock signal that is after CTS stage normal signal routing is performed. Depending on algorithm and constrain applied tool tries to optimize. After complete routing of clock, power and signal nets formal verification is performed to make sure that design is consistent with RTL.

I. Design Verification

Design rule checks (DRC), Electronic rule checks (ERC) and LVS come under design verification. Checking of maximum fan-out, shorts between ground and supply net comes under ERC check. DRC checks various design rules. Various types of design rules are DFI Integra, ipall violation, cross via violations, gnac cell violations, density cell violation, off grid violations etc. At boundary of every soc certain patterns of routing has to be followed by designer DFI Integra checks these kind of violations. For protection of chip from sudden voltage variation diodes are placed at input and output pins gnac cell violation checks these kind of violations. Routing net should be on grid off grid violation reports these violations if nets are out off grid. It is assume not to have two vias on adjacent net in same metal layer cross via violation checks these kind of violations. Finally layout versus schematic layout indicates GDS file which contains geometric information of design in order to ensure proper functionality it is compared with net list. After fixing all violation design is ready for masking.

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III. RESULTS

A. *LVS Clean Results*

Figure 3 shows result for layout versus schematic mismatch. Initially there were around 600 shorts and few opens.

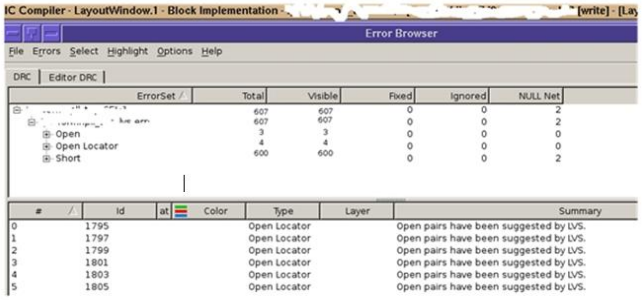

Figure 3: LVS Error Report

Figure 4 shows LVS report after fixing all shorts and opens. There are two shorts with NULL nets which are acceptable.

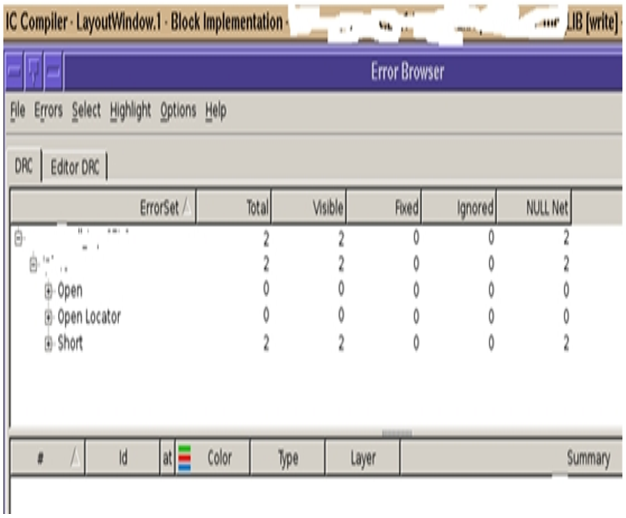

Figure 4: LVS Clean Report

B. DRC Report

Initially there are near about 4500 DRC violation. Before fabrication of any chip it is compulsory to fix all DRC. Figure 5 shows DRC error report.

Figure 5: DRC Error Report

Figure 6: DRC clean reports

C. Area Report

Figure 7 shows area report for design.

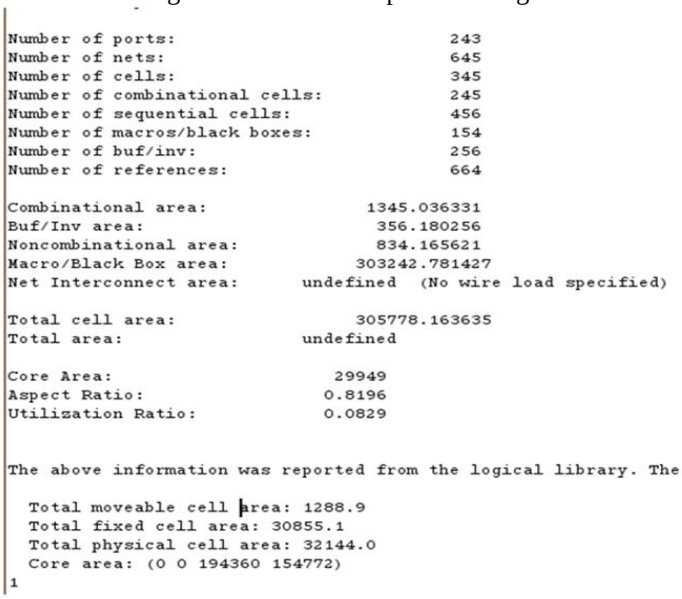

Figure 7: Area Report

D. Design quality checker report

Sr. No	Rule Name	No of Violations	Level
1	BigWireDelay	0	Warning
2	CheckAttributeConflict	0	Error
3	ClkShortedMacroEnb	0	Error
4	ClockCellOnDataPath	1	must
5	ClockDefCheck	0	Error
6	ClockNetworkRCDelay	0	must
7	ClockPropCheck	0	Error
8	ClockToSequentialDataPin	0	Error
9	DanglingInNet	45	Error
10	GateConnectedToVcc	0	Error
11	GnacOnPad	0	must
12	IllegalCells	13	Error
13	InterfaceCapTooHigh	91	Error
14	InterfacePortConnectedToLatch	0	Error
15	LogicOnClockPath	2	Error
16	LogicOnResetPathByComb	967	Error
17	MissingClockOnDualClockCells	0	Error
18	MultilevelClockGating	0	Error
19	MuxSelFromSeq	0	must
20	OutputPinsDriveSupply	0	Error
21	PwrGateTiedToConst	0	Error
22	ShortedGateOutput	0	Error
23	SideBranchOnOutput	0	must
24	SmallClockCells	0	Error
25	WrongGatedClockColor	4	Error

Fig 8: Initial Design quality checker report with Violations

Sr. No	Rule Name	No of Violations	Level
1	BigWireDelay	0	Warning
2	CheckAttributeConflict	0	Error
3	ClkShortedMacroEnb	0	Error
4	ClockCellOnDataPath	0	must
5	ClockDefCheck	0	Error
6	ClockNetworkRCDelay	0	must
7	ClockPropCheck	0	Error
8	ClockToSequentialDataPin	0	Error
9	DanglingInNet	0	Error
10	GateConnectedToVcc	0	Error
11	GnacOnPad	0	must
12	IllegalCells	0	Error
13	InterfaceCapTooHigh	10	Error
14	InterfacePortConnectedToLatch	0	Error
15	LogicOnClockPath	0	Error
16	LogicOnResetPathByComb	0	Error
17	MissingClockOnDualClockCells	0	Error
18	MultilevelClockGating	0	Error
19	MuxSelFromSeq	0	must
20	OutputPinsDriveSupply	0	Error
21	PwrGateTiedToConst	0	Error
22	ShortedGateOutput	0	Error
23	SideBranchOnOutput	0	must
24	SmallClockCells	0	Error
25	WrongGatedClockColor	0	Error

Fig 9: Design quality checker report after Violation fixes

E. Timing report

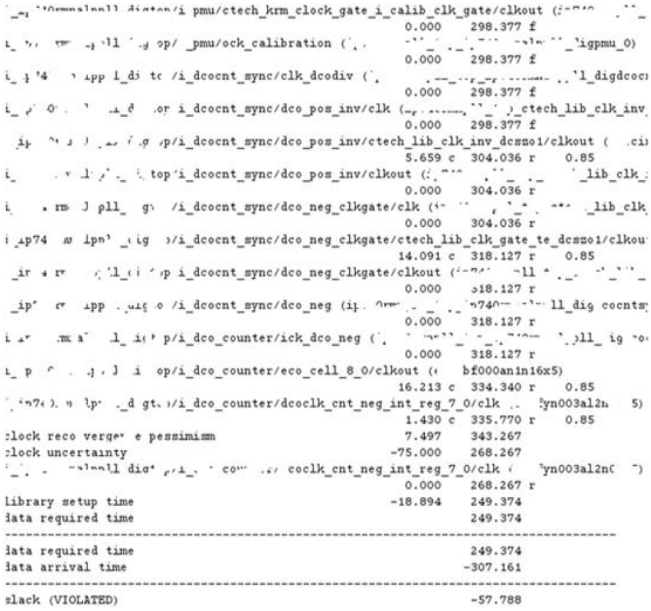

Figure 10: Setup time report with Violations

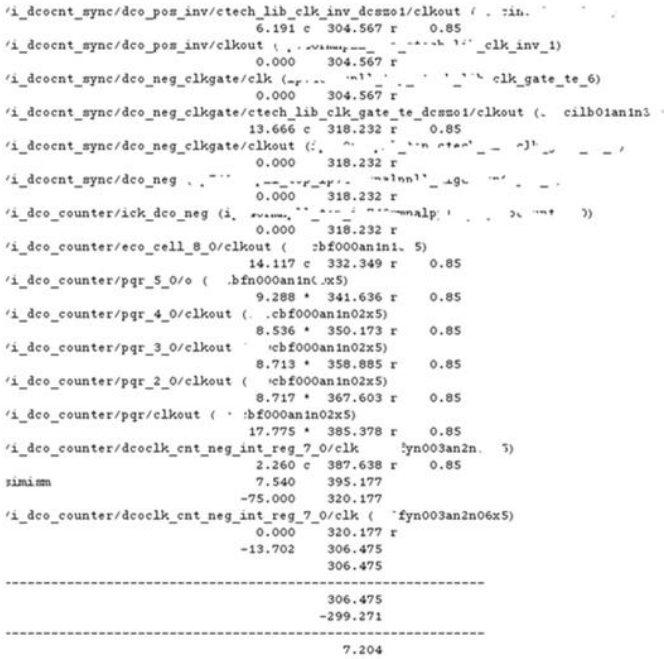

Figure 11: Setup Timing Report after Fixing Violations

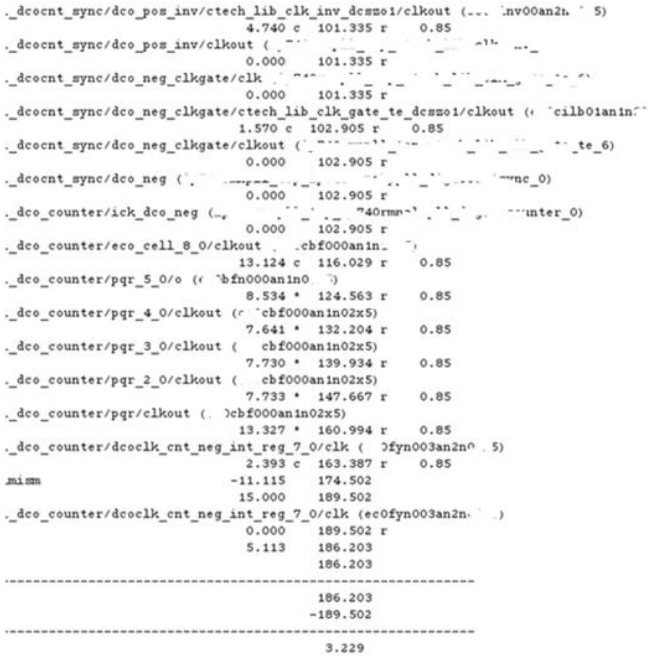

Figure 12: Hold Timing Report after Fixing Violations

IV. CONCLUSION

In this work complete physical design flow is studied. Each physical design step is performed on mixed signal IP block. Some automation tools are used in order to make design error free. Design is ready for tape out and results are found to be satisfying.

V. FUTURE ENHANCEMENT

Time to market plays an important role in any industry. In this work tools like ICC, Primetime, Design Compiler form Synopsys are used. As design size is very large tool is taking too long to complete the flow. In order to reduce this turnaround time ICC2 from Synopsys can be used. Also it is Possible to perform some more automation for fixing timing violation which may help in improving turnaround time as well as accuracy.

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